Express Mail Label No. EL 569 075 024 US

7-31-00 A

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 11675.76.1.1

Total Pages in this Submission 23

JC895 U.S. PTO 07/28/00

JC895 U.S. PTO 09/627381 07/28/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME

and invented by:

Gurtej S. Sandhu, Anand Srinivasan and Ravi Iyer

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **09/249,659**

Which is a:

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **08/677,514**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **23** pages and including the following:

a. ☒ Descriptive Title of the Invention
b. ☒ Cross References to Related Applications *(if applicable)*
c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
d. ☐ Reference to Microfiche Appendix *(if applicable)*
e. ☒ Background of the Invention
f. ☒ Brief Summary of the Invention
g. ☒ Brief Description of the Drawings *(if drawings filed)*
h. ☒ Detailed Description
i. ☒ Claim(s) as Classified Below
j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
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Docket No.
11675.76.1.1
Total Pages in this Submission
23

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 5
   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing
   ☐ First Class ☒ Express Mail *(Specify Label No.):* EL 569 075 024 US

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
11675.76.1.1
Total Pages in this Submission
23

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	34	- 20 =	14	x	$18.00	$252.00
Indep. Claims	5	- 3 =	2	x	$78.00	$156.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)*						$0.00
					TOTAL FILING FEE	$1,098.00

☒ A check in the amount of see form PTO-2038 to cover the filing fee is enclosed.

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Signature

Bradley K. DeSandro, Reg. No. 34,521

Dated: July 21, 2000

22901

PATENT TRADEMARK OFFICE

cc:

TRANSMITTAL LETTER (General - Patent Pending)	Docket No. 11675.76.1.1

In Re Application Of: **Sandhu et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
Not yet assigned	**Herewith**	**Not yet assigned**	**Not yet assigned**

Title: **INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Utility Patent Application Transmittal Letter (3 pgs); Divisional Pat. App. (23 pgs); Five (5) Sheets of Formal Drawings; Assignment; Declaration; Form PTO-2038; Certificate of Mailing by Express Mail No. EL 569 075 024 US; Postcard

in the above identified application.

- ☐ No additional fee is required.
- ☒ A check in the amount of see form PTO-2038 is attached.
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Dated: **July 27, 2000**

Bradley K. DeSandro, Reg. No. 34,521

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Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Sandhu et al.**	Docket No. **11675.76.1.1**

Serial No.	Filing Date	Examiner	Group Art Unit
Not yet assigned	**Herewith**	**Not yet assigned**	**Not yet assigned**

Invention: **INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME**

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(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

July 28, 2000
(Date)

Peggy R. Huft
(Typed or Printed Name of Person Mailing Correspondence)

Peggy R. Huft
(Signature of Person Mailing Correspondence)

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Note: Each paper must have its own certificate of mailing.

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APPLICATION INFORMATION

Title Line One:: INTERLEVEL DIELECTRIC STRUCTURE AND METH
Title Line Two:: OD OF FORMING SAME
Total Drawing Sheets:: 5
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: 11675.76.1.1
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 22901
Registration Number One:: 34521

CONTINUITY INFORMATION

This application is a:: DIVISION OF
> Application One:: 09/249,659
Filing Date:: 02-12-1999

Which is a::DIVISION OF
>> Application Two:: 08/677,514
Filing Date:: 07-10-1996

Source:: PrintEFS Version 1.0.1

Express Mailing Label No. EL 569 075 024 US Docket No. 11675.76.1.1

UNITED STATES PATENT APPLICATION

of

GURTEJ S. SANDHU

ANAND SRINIVASAN

and

RAVI IYER

for

INTERLEVEL DIELECTRIC STRUCTURE AND METHOD OF FORMING SAME

1. Related Applications

This application is a divisional of application serial number 09/249,659, filed on February 12, 1999, which is a divisional application of serial number 08/677,514, filed on July 10, 1996, titled Interlevel Dielectrics and Methods for Forming the Same, both of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

2. The Field of the Invention

The present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices. More particularly, the present invention relates to the design and manufacture of interlevel dielectrics in the manufacture of semiconductor devices in which the dielectric constant of the interlevel dielectric is less than about 3.6.

3. The Relevant Technology

The continuing trend in the semiconductor industry of squeezing more and more circuit devices into a given area has resulted in significant improvements in the performance of individual integrated circuits and of electronic devices that employ integrated circuits. In a typical integrated circuit, individual circuit elements or groups of elements are generally electrically connected together by a metallization process, in which layers of metal are deposited and patterned to form metal lines which complete the circuit as designed. Multiple metal layers are often employed. Metal lines within patterned metal layers are insulated by layers known as interlevel dielectrics. The interlevel dielectrics insulate the metal lines from any undesired electrical contact both with other metal lines, whether in the same or another metal layer, and with other circuit elements.

The capacitance between two conductive materials is also affected by the material as well as the distance between them. The ratio of the capacitance between two conductors with a given material between them to the capacitance of the same two conductors with

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nothing (a vacuum) between them is known as the dielectric constant of the given material. Thus a material with a high dielectric constant placed between two conductors increases the capacitance between the two conductors.

The increasing density of integrated circuits has resulted in unneeded capacitance between metal lines in an integrated circuit due to metal line coupling capacitance. The unneeded capacitance slows circuit performance by causing too much buildup of charge where none is needed, thus slowing the buildup of charge at circuit elements where it is needed.

One way to decrease unneeded capacitance between metal lines in an integrated circuit is to decrease the dielectric constant of the material between them. Silicon dioxide, the material of choice for interlevel dielectrics, has a relatively high dielectric constant. Replacing silicon dioxide with a material having a lower dielectric constant would thus provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to reliably protect the metal lines, and are unable withstand further processing.

One way to gain some of the benefits of low dielectric constant materials is shown in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal, overlie first dielectric layer 14. A material with a dielectric constant lower than that of silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive material 16 together with low dielectric constant dielectric material 18 are covered by a second dielectric layer 21 comprised of a traditional dielectric material such as silicon dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low dielectric constant dielectric material 18 from other portions of the integrate circuit. Second

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dielectric layer 21 allows further processing, including formation of contact holes for contacting lines of conductive material 16 such as contact hole 46, without exposing dielectric material 18 to processing agents.

While the structure shown in Figure 1 results in decreased capacitance between adjacent pairs of metal lines, further decrease is needed to allow increasing miniaturization and high speed operation of ever denser integrated circuits.

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SUMMARY OF THE INVENTION

In accordance with the present invention, an interlevel dielectric structure includes first and second dielectric layers between which are located lines of a conductive material with a dielectric material in spaces between the lines of conductive material, with the lower surface of the dielectric material extending lower than the lower surface of lines of conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of lines conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing.

A preferred method for forming the interlevel dielectric structure includes providing an additional layer on a conductive layer on a first dielectric layer, then patterning both the additional layer and the conductive layer with an over etch into but not through the first dielectric layer, to form conductive lines with spaces therebetween. A dielectric material is then deposited to fill the spaces and is then etched or chemically mechanically polished back to the additional layer on the conductive layer. The additional layer on the conductive layer is then optionally removed before a second dielectric layer is deposited over all.

Another preferred method for forming the interlevel dielectric structure includes providing a conductive layer on a first dielectric layer, then patterning the conductive layer with an over etch into but not through the first dielectric layer to form conductive lines with spaces therebetween. An additional layer is then deposited by a method providing poor step coverage. The additional layer is then optionally etched, and a dielectric material is then deposited in the spaces. The dielectric material is then etched or chemically mechanically

polished back to the additional layer. The additional layer is then optionally removed before a second dielectric layer is deposited over all.

Yet another preferred method for forming the interlevel dielectric structure includes providing a metal layer on a first dielectric layer, then patterning the metal layer with an over etch into but not through the first dielectric layer to form metal lines with spaces therebetween. A thin layer of silicon dioxide is then deposited by a method providing preferential deposition on the upper surfaces of the metal lines. The thin layer of silicon dioxide is then optionally etched, and a dielectric material is then deposited to fill the spaces and is then etched or chemically mechanically polished back. A second dielectric layer is then deposited over all.

The above briefly described methods allow reliable formation of a desired interlevel dielectric structure, which structure provides reduced total capacitance between adjacent conductive lines needed for further miniaturization of integrated circuits.

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BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained may be more fully explained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments and applications thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments and applications of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross section of a partially formed integrated circuit device.

Figure 2 is a partial cross section of a partially formed integrated circuit device having a structure formed during the practice of a method of the present invention.

Figure 3 is a partial cross section of a partially formed integrated circuit device for use with a method of the present invention.

Figure 4 is a cross section of the structure shown in Figure 3 after further processing, and having a structure formed by a method of the present invention.

Figure 5 is a partial cross section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

Figure 6 is a partial cross section of a partially formed integrated circuit device depicting facet etching of a bread-loafed dielectric on metallization lines.

Figure 7 is a cross section of the structure shown in Figure 5 after further processing, and having a structure formed by a method of the present invention.

Figure 8 is a partial cross section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

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Figure 9 is a cross section of the structure shown in Figure 8 after further processing, having a structure formed by a method of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention introduces an interlevel dielectric structure having a dielectric material between conductive lines with a lower surface of the dielectric material below a lower surface of the conductive lines, and an upper surface of the dielectric material above an upper surface of the conductive lines. The present invention also provides various methods for constructing the inventive structure. Because silica glass is used extensively in this art as a dielectric, and its dielectric constant is about 3.8, we define the interlevel dielectric material as one having a dielectric constant below about 3.6, preferably below about 2.9, and most preferably below about 2.2.

A preferred embodiment of the structure of the present invention is shown in Figure 2. A substrate or underlying layer(s) 12 of a semiconductor device is overlaid with a first dielectric layer 14, typically comprised of silicon dioxide, and having an upper surface 22. Lines of conductive material 16 with spaces therebetween extend (perpendicular to the plane of Figure 2) along upper surface 22 of first dielectric layer 14. Each of the lines of conductive material 16 has a lower surface 24 and an upper surface 26, with lower surfaces 24 being in contact with upper surface 22 of first dielectric layer 14. Lines of conductive material 16 are typically metal such as aluminum or copper, but may be comprised of other conductive materials such as polysilicon, aluminum, copper, tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations thereof.

A second dielectric layer 20 overlies lines of conductive material 16, with a lower surface 28 of second layer of dielectric material 20 being in contact with upper surfaces 26 of lines of conductive material 16.

Dielectric material 17, comprised of polytetrafluoroethylene (PTFE) or other suitable material, is situated in the spaces between lines of conductive material 16. Dielectric material 17 has an upper surface 32 higher than the upper surfaces 26 of lines of conductive

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material 16 adjacent thereto, and a lower surface 30 lower than the lower surfaces 24 of lines of conductive material 16 adjacent thereto.

The extension of dielectric material 17 below and above lines of conductive material 16 significantly reduces capacitance between adjacent pairs of lines of conductive material 16.

The electric field formed by a potential difference applied across an adjacent pair of lines of conductive material 16 is strongest in a direct line and centrally between the adjacent pair, such as along dashed line N in Figure 2. But the electric field so formed also extends to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in Figure 2. The field in this area, called the fringe, is associated with a portion of the total capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

The portion of the total capacitance included in fringe capacitance increases as aspect ratio (height/width) of lines of conductive material 16 decreases, and can be a significant fraction of total capacitance at low aspect ratios. The extension of dielectric material 17 below and above lines of conductive material 16 provides a low dielectric material in the fringe areas of the electric field, thus reducing fringe capacitance and total capacitance accordingly.

While dielectric material 17 extends below and above lines of conductive material 16, it does not extend directly over surface 26 or under surface 24. This allows formation of contact holes such as contact hole 48 without exposing dielectric material 17 to processing agents that could degrade dielectric material 17 or upper surface 26 at contact hole 48.

The above structure and variations thereon may be formed in a variety of ways, presently preferred examples of which will be described below.

One preferred method of forming a structure of the present invention includes providing a first dielectric layer 14 over the surface of a substrate of an underling layer 12,

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then forming a conductive layer 34 and an additional layer 36 thereover, as shown in Figure 3. Conductive layer 34 and additional layer 36 are then patterned by forming and patterning a mask layer over additional layer 36, and then etching additional layer 36, conductive layer 34, and a portion of first dielectric layer 14 at areas that are left exposed through the mask layer. This results in spaces between adjacent remaining portions of conductive layer 34.

Dielectric material 17 is then deposited to fill these spaces, and then removed from the top downward to at least the top of the remaining portions of additional layer 36 by an etch back or by chemical mechanical polishing. A second dielectric layer 21 is then deposited over the substrate, resulting in the structure shown in Figure 4.

In Figure 4, lines of conductive material 16 are formed of the remaining portions of conductive layer 34. Dielectric material 17 is deposited between lines of conductive material 16. If additional layer 36 is comprised of a suitable dielectric such as silicon dioxide, the remaining portions of additional layer 36 may be incorporated into the inventive structure as shown. Thus the remaining portion of additional layer 36 in Figure 4, together with second dielectric layer 21, correspond to the depiction seen in Figure 2 as second dielectric layer 20.

If additional layer 36 is not a dielectric, such as if titanium is used, for example, then the remaining portions of layer 36 shown in Figure 4 are removed by an appropriate process immediately before the deposition of second dielectric layer 20. This alternative additional process step results in a structure like that which is shown in Figure 2.

Another preferred method of forming a structure of the present invention includes providing a first dielectric layer over a substrate or an underlying layer, then depositing and patterning a conductive layer over the first dielectric layer. During patterning of the conductive layer, the conductive layer is over etched such that the first dielectric layer is

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etched partially with the same pattern. Next, an additional layer is deposited over the patterned metal layer by a deposition method having poor step coverage.

The results of the above steps are shown in Figure 5. First dielectric layer 14 has been formed on substrate or underlying layer 12, and a conductive layer has been deposited and patterned, leaving lines of conductive material 16. Additional layer 38 has been deposited by a deposition method having poor step coverage. This results in additional layer 38 being formed substantially only on the upper surfaces of lines of conductive material 16 as shown.

If additional layer 38 is comprised of a suitable dielectric material, the further process steps may proceed as before, with deposition and partial top-down removal of dielectric material 17 and deposition of second dielectric layer 21, resulting in the structure shown in Figure 7. The remaining portions of additional layer 38 are incorporated into the inventive structure as shown, so that the remaining portion of additional layer 38 in Figure 5 together with second dielectric layer 21 in Figure 7, correspond to the depiction seen in Figure 2 as second dielectric layer 20.

Silicon dioxide is the currently preferred material for additional layer 38, with deposition by a silane and oxygen plasma enhanced chemical vapor deposition (PECVD) being the preferred poor step coverage deposition method.

Figure 6 illustrates an optional etch step that may be included immediately after deposition of additional layer 38 to remove lateral buildup of additional layer 38. The preferred etch is a facet etch, and is preferably performed in an argon or an argon-plus-fluorine based plasma. In a facet etch, additional layer 38 is etched slower at a top surface thereof than it is etched at a corner thereof which connects the top surface to a lateral surface thereof. The facet etch has the effect of removing substantially all of the lateral buildup portions of additional layer 38 and the removed portions redeposit in semi-triangular form

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at the base of the lines of conductive material 16 and first dielectric layer 14 interface. A continuous but thin lateral layer of additional layer 38 also deposits down the sides of lines of conductive material 16. Further processing as above then results in a structure like that which is shown in Figure 4, with the remaining portions of layer of additional material 36 corresponding to the remaining portions of additional layer 38. The redeposited fraction of additional material 38, however, remains thinly on the sides of lines of conductive material 16 and first dielectric layer 14.

If additional layer 38 is not a dielectric, or is otherwise not suitable to remain in place in the inventive structure, then additional layer 38 is removed by an appropriate process immediately before the deposition of second dielectric layer 21. This alternative additional process step results in a structure that is like that shown in Figure 2.

In yet another presently preferred method for forming a structure of the present invention, a first dielectric layer is provided over a substrate or an underlying layer, then a metal layer is deposited and patterned to form metal lines over the first dielectric layer. During patterning of the metal layer, the metal layer is over etched such that the first dielectric layer is etched partially with the same pattern. A thin silicon dioxide layer is then deposited conformably over the metal lines by a deposition process that deposits preferentially on the upper surface of the metal lines.

The above process results generally in the structure shown in Figure 8. First dielectric layer 14 is formed on substrate 12. Metal lines in the preferred form of aluminum lines 40 have been formed on first dielectric layer 14, and first dielectric layer 14 has been over etched in the same pattern as aluminum lines 40. A titanium nitride film 42 from a photolithography process used to pattern aluminum lines 40 remains on the upper surface of aluminum lines 40. While not required, inclusion of titanium nitride film 42 is presently preferred.

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The preferred deposition process for selectively depositing a thin silicon dioxide layer 44 is an ozone based TEOS process, which preferentially deposits on TiN over silicon dioxide. Preferably, silicon dioxide layer 44 will be deposited only on titanium nitride film 42 and not on the sidewall of aluminum lines 40 as shown in Figure 8.

After deposition of silicon dioxide layer 44, the process may continue as with the other above processes by deposition and partial removal of a dielectric material 17, followed by deposition of second dielectric layer 21, resulting in the structure shown in Figure 9. Silicon dioxide layer 44 is incorporated into the inventive structure as shown, so that silicon dioxide layer 44 together with second dielectric layer 21 correspond to the depiction seen in Figure 2 as second dielectric layer 20.

As an alternative process step, an etch such as a facet etch in an argon or an argon-plus-fluorine based plasma may be performed on silicon dioxide layer 44 after the deposition thereof.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

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1. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer;

depositing an additional layer on said conductive layer;

patterning said conductive layer and said additional layer by

forming a patterned mask layer on said additional layer, and

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

2. The method as defined in Claim 1, further comprising the step, to be performed after said step of removing said layer of dielectric material and before said step of depositing a second dielectric layer, of removing said additional layer on said lines of conductive material.

3. The method as defined in Claim 2, wherein said additional layer comprises titanium.

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4. The method as defined in Claim 2, wherein said additional layer comprises TiN.

5. The method as defined in Claim 1, wherein at least one said first and second dielectric layers comprises silicon dioxide.

6. The method as defined in Claim 1, wherein said dielectric material comprises PTFE.

7. The method as defined in Claim 1, wherein said additional layer comprises silicon dioxide.

8. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises an etch back step.

9. The method as defined in Claim 1, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

10. The method as defined in Claim 1, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations thereof.

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11. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situates on a semiconductor wafer;

depositing a conductive layer on said first dielectric layer;

patterning said conductive layer by

forming a mask layer on said conductive layer, and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

12. The method as defined in Claim 11, wherein depositing an additional layer comprises depositing a layer of silicon dioxide by silane and oxygen based plasma enhanced chemical vapor deposition.

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13. The method as defined in Claim 11, further comprising, after depositing an additional layer and before depositing a layer of dielectric material, of etching said additional layer.

14. The method as defined in Claim 13, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

15. The method as defined in Claim 13, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

16. The method as defined in Claim 11, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

17. The method as defined in Claim 11, wherein said dielectric material comprises PTFE.

18. The method as defined in Claim 11, wherein said additional layer comprises silicon dioxide.

19. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises an etch back step.

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20. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

21. The method as defined in Claim 11, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, and copper.

22. A method of forming an interlevel dielectric comprising the steps of:

providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;

depositing a metal layer on said first dielectric layer;

patterning said metal layer by

forming a mask layer on said metal layer, and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;

removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and

depositing a second dielectric layer over all layers on said surface of said substrate.

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23. The method as defined in Claim 22, wherein said step of depositing a layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines comprises an ozone-based TEOS deposition.

24. The method as defined in Claim 22, wherein said metal lines comprise aluminum with a titanium nitride film on said upper surface of said metal lines.

25. The method as defined in Claim 22, further comprising, after depositing a layer of silicon dioxide conformably over said metal lines and before depositing a layer of dielectric material, of etching said additional layer.

26. The method as defined in Claim 25, wherein said additional layer has a top surface extending to a lateral surface at a corner, and wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer.

27. The method as defined in Claim 26, wherein said additional layer comprises silicon dioxide and wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma.

28. The method as defined in Claim 22, wherein at least one of said first and second dielectric layers comprises silicon dioxide.

29. The method as defined in Claim 22, wherein said dielectric material comprises PTFE.

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30. The method as defined in Claim 22, wherein said additional layer comprises silicon dioxide.

31. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises an etch back step.

32. The method as defined in Claim 22, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.

33. The method as defined in Claim 22, wherein said metal layer comprises at least one of aluminum or copper.

34. A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer;

forming an additional layer on said conductive layer;

forming lines of conductive material having spaces therebetween from the conductive layer;

filling the spaces between the lines of conductive material with dielectric material having a dielectric constant of less than about 3.6;

forming a second dielectric layer on the additional layer.

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35. A method of forming an interlevel dielectric comprising:

providing a first dielectric layer over a surface of a substrate;

forming a conductive layer on said first dielectric layer;

forming an additional layer on said conductive layer;

etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;

filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6;

forming a second dielectric layer on the additional layer.

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ABSTRACT OF THE INVENTION

An interlevel dielectric structure includes first and second dielectric layers between which are located lines of a conductive material with a dielectric material in spaces between the lines of conductive material, with the lower surface of the dielectric material extending lower than the lower surface of lines of conductive material adjacent thereto, and the upper surface of the dielectric material extending higher than the upper surface of conductive material adjacent thereto, thus reducing fringe and total capacitance between the lines of conductive material. The dielectric material, which has a dielectric constant of less than about 3.6, does not extend directly above the upper surface of the lines of conductive material, allowing formation of subsequent contacts down to the lines of conductive material without exposing the dielectric material to further processing. Various methods for forming the interlevel dielectric structure are disclosed.

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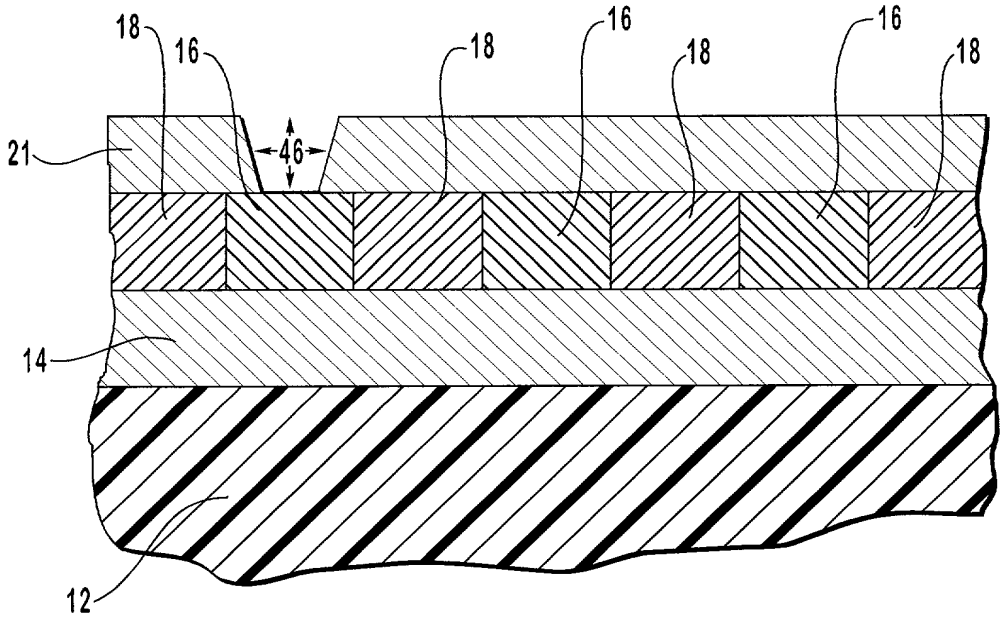

FIG. 1
(PRIOR ART)

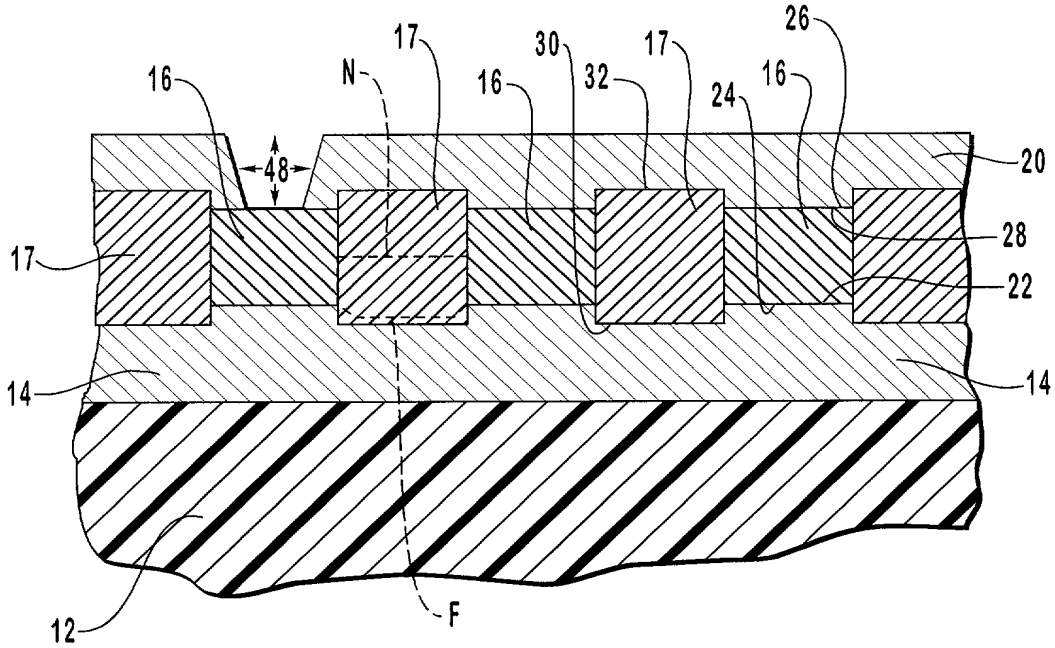

FIG. 2

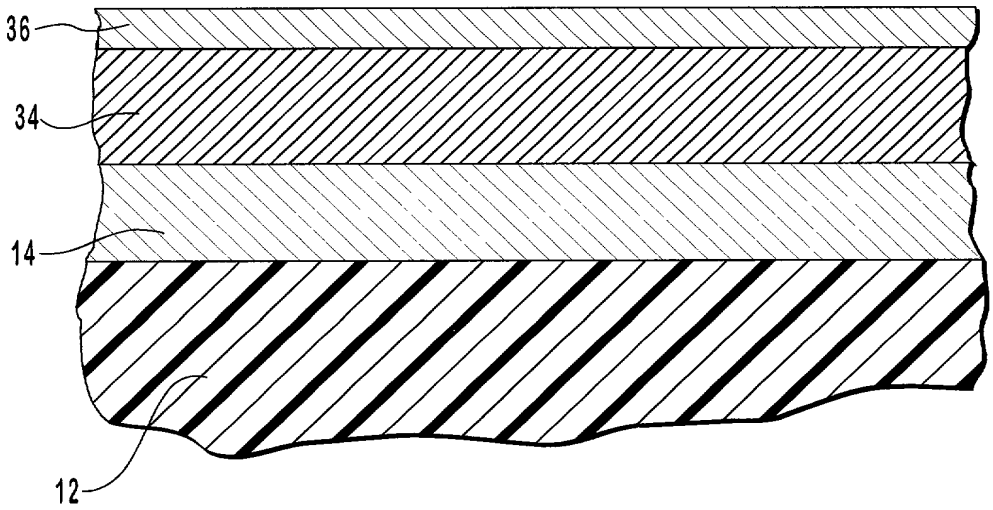

FIG. 3

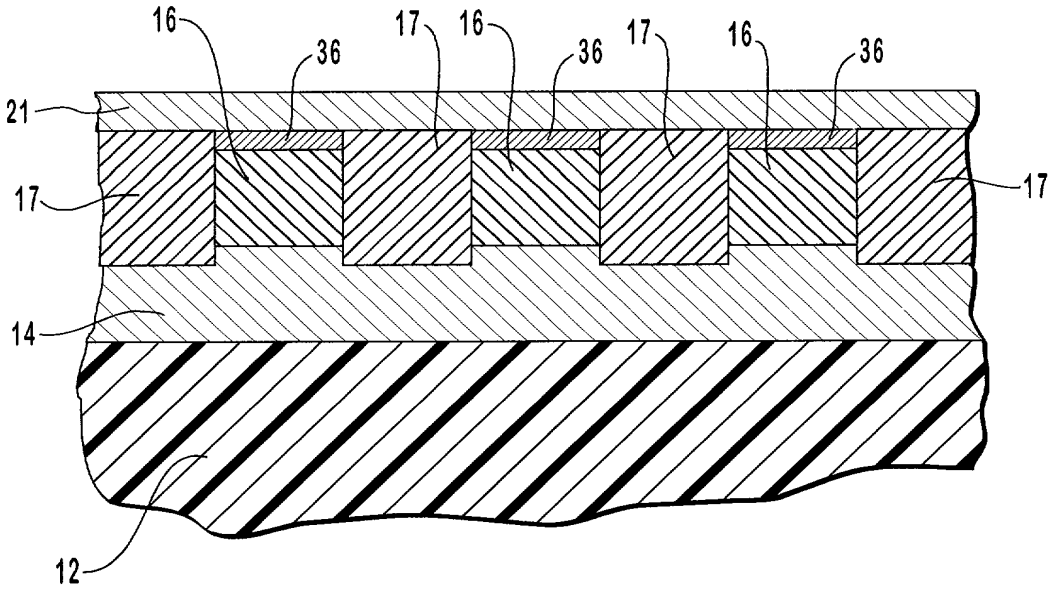

FIG. 4

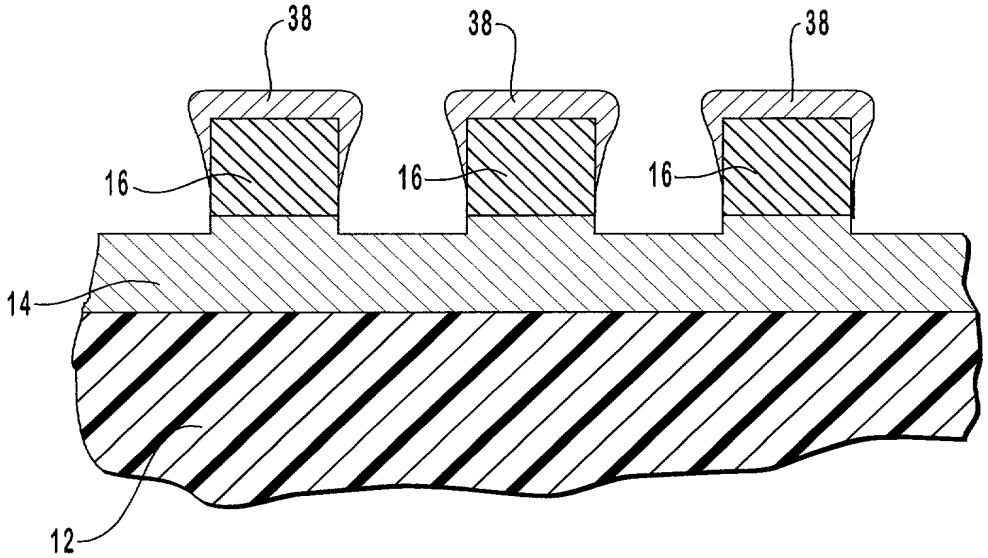

FIG. 5

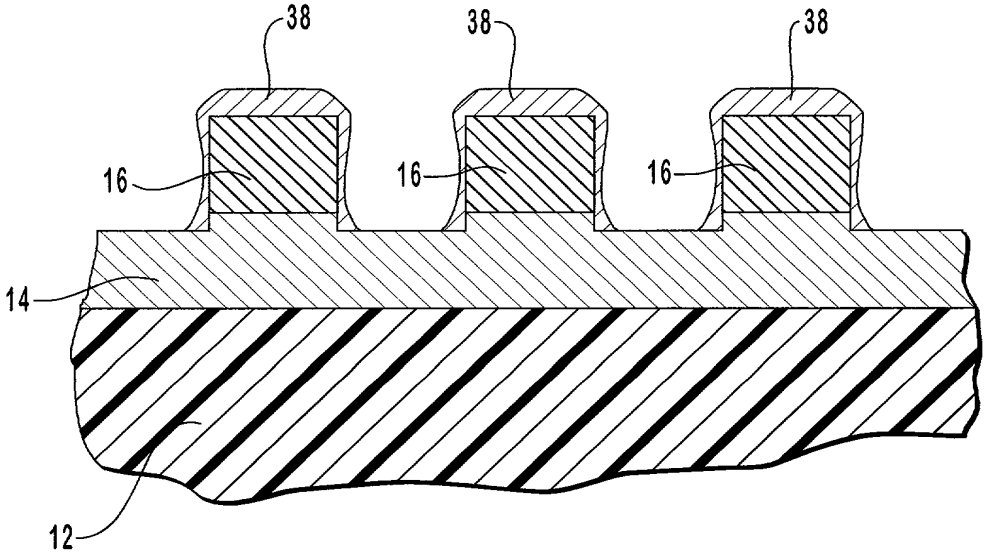

FIG. 6

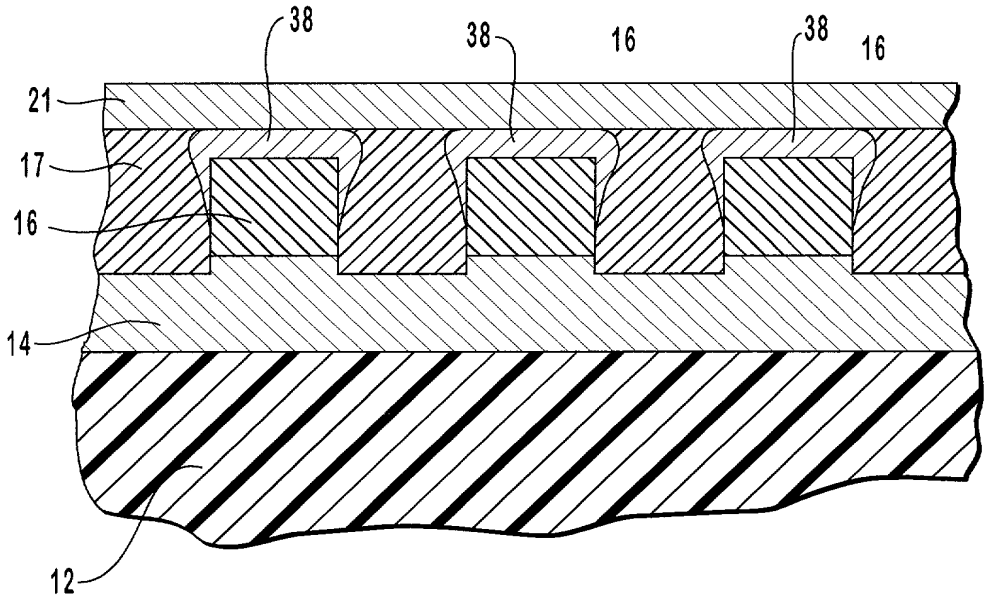

FIG. 7

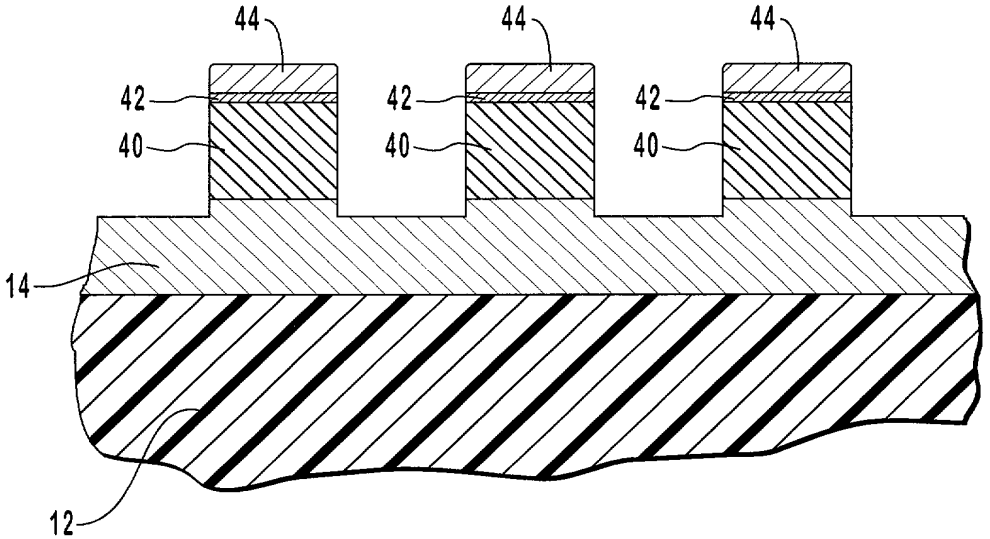

FIG. 8

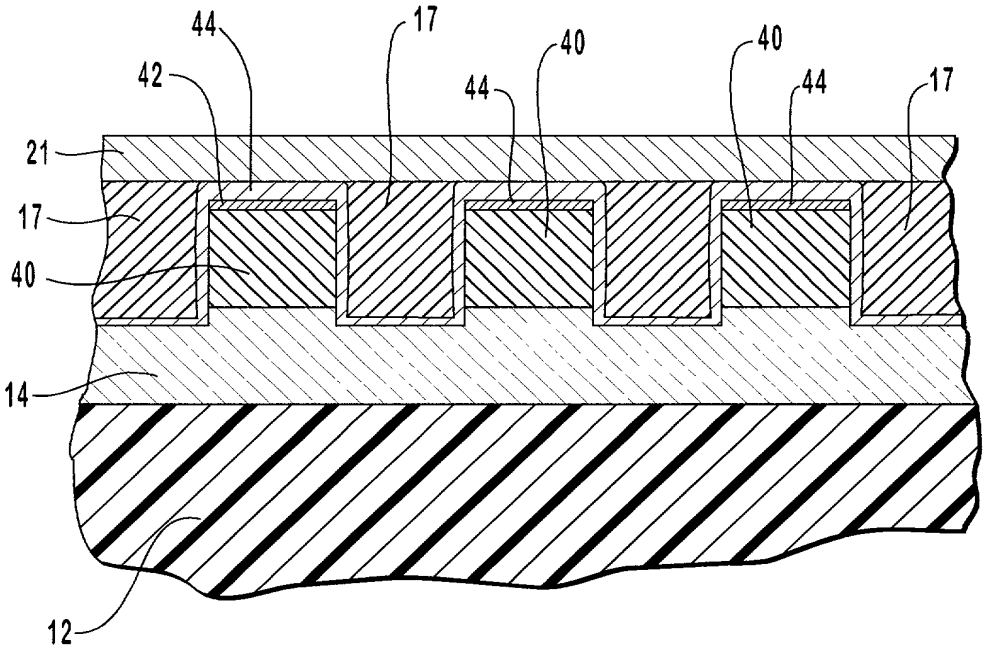

FIG. 9

PATENT APPLICATION
Docket No: 11675.76

DECLARATION, POWER OF ATTORNEY, AND PETITION

We, Gurtej Sandhu, a citizen of the United Kingdom, Anand Srinivasan, a citizen of India, and Ravi Iyer, a citizen of India, declare: that we are citizens as stated above; that our residences and post office addresses are 2964 East Parkriver Drive, Boise, Idaho, 83706, 670 South Clearwater, #201, Boise, Idaho, 83712, and 5600 South Fuchsia, Boise, Idaho, 83705, respectively; that we verily believe we are the original, first, and joint inventors of the subject matter of the invention or discovery entitled INTERLEVEL DIELECTRIC STRUCTURE AND METHODS FOR FORMING THE SAME for which a patent is sought and which is described and claimed in the specification attached hereto; that we have reviewed and understand the contents of the above-identified specification, including the claims referred to, and that we acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

We hereby appoint as our attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; KENT S. BURNINGHAM, Registration No. 30,453; TODD E. ZENGER, Registration No. 33,610; JONATHAN W. RICHARDS, Registration No. 29,843; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; DANA L. TANGREN, Registration No. 37,246; ERIC L. MASCHOFF, Registration No. 36,596; GREGORY M. TAYLOR, Registration No. 34,263; KEVIN B. LAURENCE, Registration No. 38,219; JOHN N. GREAVES, Registration No. P-40,362; BRIAN C. KUNZLER, Registration No. 38,527; JEFFREY L. RANCK, Registration No. 38,590; LENA I. VINITSKAYA, Registration No. 39,448; LIA M. PAPPAS, Registration No. 34,095; and MICHAEL L. LYNCH, Registration No. 30,871, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith. All correspondence and telephonic communications should be directed to:

BRADLEY K. DeSANDRO
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, we pray that Letters Patent be granted to us for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 5th day of July, 1996.

Inventor: ______________________

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Signed at BOISE, Idaho, this 5th day of JULY, 1996.

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